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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,278	11/24/2003	Munehiro Ito	P/29-1642	8776

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EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 03/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,278	ITO, MUNEHIRO	
	Examiner	Art Unit	
	John P. Trimmings	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☒ Claim(s) *1,5,7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/24/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-9 are presented for examination.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

2. Should applicant desire to obtain the benefit of foreign priority under 35 U.S.C. 119(a)-(d) prior to declaration of an interference, a translation of the foreign application should be submitted under 37 CFR 1.55 in reply to this action.

3. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 11/29/2002. It is noted, however, that applicant has not filed a certified copy of the translation of the application as required by 35 U.S.C. 119(b)(3). Therefore, the examiner will not recognize the priority date when submitting comparable references.

Information Disclosure Statement

4. The examiner has not considered the Information Disclosure Statement under "Other Documents" because the applicant did not provide the purported English-language translation.

However, through USPTO resources, an acceptable unofficial translation was obtained, and so the examiner has considered the entry under "Foreign Patent Documents".

Drawings

5. The drawing in FIG.1 is objected to under 37 CFR 1.83(a) because it fails to show IDT and ICK as described in the specification on pages 2, 3 and 4.

6. The drawing in FIG.3 is objected to under 37 CFR 1.83(a) because it fails to show EAD and PCK as described in the specification on pages 9 and 10.

7. The drawings are objected to under 37 CFR 1.83(a) because they fail to show "WCM" and "RCM" as described in the specification, page 8 and 9.

8. FIG.8 and the disclosure, pages 21 through 28 describe addressing and data that are related, where the EAD is (2,0), (3,0), (0,0) and (1,0), but FIG.8 illustrates the IAD to be (0,0), (1,0), (2,0) and (3,0) for each LAD. This is contrary to the teachings in the disclosure wherein the IAD is column addressing and EAD/LAD is row addressing. According to the applicant's drawing and other teachings, the IAD under EAD=(2,0) should be (2,0), (2,1), (2,2) and (2,3), and not as shown; (0,0), (1,0), (2,0) and (3,0). The examiner has conceived the invention to be different to that which is disclosed and illustrated. The examiner requests that the applicant specifically explains the discrepancies in the

examiner's conception of the applicant's invention, and make the necessary changes to create a clear disclosure and drawing, as required.

Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

9. The disclosure is objected to because of the following informalities:

a. Page 2 line 17 should be corrected to recite, "... In ~~tenting~~ testing ...".

b. Page 2 lines 16, 20 and 23, and page 3 line 1, and page 4 line 17 refer to "ICK" in FIG.1 but the signal is named "CK" in the figure. The examiner requests correction.

c. Page 2 line 25 refers to "IDT" in FIG.1 but the signal is named "DT" in the figure. The examiner requests correction.

d. Page 8 lines 8, 10, 22 and 26, and page 9 line 21 refer to signals "RCM" and "WCM" not depicted in the drawings. The examiner requests correction.

e. Page 9 lines 20, 26, and page 10 lines 3, 6, 13, 18, 23, and 25 refer to signals "EAD" and "PCK". The examiner requests that the herein references be coordinated with the drawing of FIG.3.

f. Page 9 lines 5-10 describe the x,y representation of the internal address IAD as; x being a 4-bit row address, and y being a 4-bit column address. But in order to generate "four internal addresses" (page 10 line 2) for IAD, the size of the example described should be x = 2-bit row address and y = 2-bit column address. Also, if EAD is (2,0) as described, and the example should recite, "the four internal addresses IAD are (2,0), 2,1), (2,2) and 2,3).". The examiner requests that appropriate correction be returned in the applicant's next communication.

g. Page 15 line 25 refers to "CD" in FIG.2 but the signal is named "CK" in the figure. The examiner requests correction.

h. Page 26 line 9 and page 28 line 24 refer to "transfer gate 66" in FIG.4 but the signal is named "transfer gate 67" in the figure. The examiner requests correction.

i. Pages 21 through 28 describe addressing and data related to FIG.8, where the EAD is (2,0), (3,0), (0,0) and (1,0), but illustrates the IAD to be (0,0), (1,0), (2,0) and (3,0) for each LAD. This is contrary to the teachings in the disclosure wherein the IAD is column addressing and EAD/LAD is row addressing. According to the applicant's drawing and other teachings, the IAD under EAD=(2,0) should be (2,0), (2,1), (2,2) and (2,3), and not as shown; (0,0), (1,0), (2,0) and (3,0). The examiner requests that the applicant specifically explains the discrepancies in the examiner's conception of the applicant's invention, and make the necessary changes to create a clear disclosure and drawing, as required.

Claim Objections

10. Claims 1 and 5 are objected to because of the following informalities: Lines 8 and 4 respectively claim, "... (n is a natural number) ...". But recitals within parenthesis do not hold patentable weight. Appropriate correction is required.

11. Claim 7 is objected to because of the following informalities: The period at the end of the claim is missing. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Line 13 instantiates a second "external address", and so the examiner is not sure if the applicant means to limit the external address of line 4, or if the applicant is limiting a second external address.

Line 15 instantiates a second "n number of internal addresses", and so the examiner is not sure if the applicant means to limit the internal addresses of line 3, or if the applicant is limiting a second internal address.

Line 16 refers to "the external address", but the examiner is not sure if the applicant means to limit the external address of line 13, or if the applicant is limiting the external address of line 4.

Lines 18 and 20 refer to "the internal addresses", but the examiner is not sure if the applicant means to limit the internal addresses of line 15, or if the applicant is limiting the internal addresses of line 3.

Line 21 refers to "the latched external address", but the examiner is not sure if the applicant means to limit the external address of line 13, or if the applicant is limiting the external address of line 4.

13. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Line 5 refers to "the latched external address", but the examiner is not sure if the applicant means to limit the external address of line 13 of Claim 1, or if the applicant is limiting the external address of line 4 of Claim 1.

14. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Line 3 refers to "the internal addresses", but the examiner is not sure if the applicant means to limit the internal addresses of line 3 of Claim 1, or if the applicant is limiting the internal addresses of line 15 of Claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 1, 2, 4-6, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kazuyuki, Japanese Patent Application No. 07-078495, in view of Haraguchi et al. (herein Haraguchi), U.S. Patent No. 6650583.

As per Claims 5 and 1:

Kazuyuki teaches a method for testing based on a test circuit for a semiconductor memory device (see Title), comprising: a high-speed clock generating circuit (see Constitution and FIG.1 PLL) which generates a high-speed clock (see Constitution) which has a frequency n times that of an external clock (in this case, n=4, see Example line 3,4) and is synchronized with the external clock (output is 4*f* of input *f*); a high-speed address generating circuit (see Constitution and FIG.1 AGU) which generates, in synchronization with the high-speed clock (see Example lines 6-8), n number (4) of first internal addresses (see FIG.1 AGU out is four addresses based on A0 and A1) including a first external address supplied (when AGU A0, A1 is 00) for designating a storage region of data (see FIG.2 where A0, A1 count up from 0) for 1 bit to be written into a storage unit of a semiconductor memory device (see Example lines 5-10), and generates n number of second internal addresses including the external address in synchronization with the high-speed clock (see Example lines 11-15 and FIG.1 and FIG.2); and a high-speed data generating circuit which generates n bits of internal write data (Example lines 1-10) corresponding to n number (4) of the first internal addresses in synchronization with the high-speed clock (using the 4*f* clock), supplies the internal write data to the storage unit (Example, lines 5-9) and outputs internal read data corresponding to one of n number (4) of the second internal addresses (see Example line 10-13), which coincides with a latch address (when A0, A1 is 00, A2-An is the latch address), out of n bits (4) of the internal read data read from the storage unit in

synchronization with the high-speed clock (Example lines 10-13). But the reference Kazuyuki fails to teach a second address (the read cycle address) as a latch address. But in the analogous art of Haraguchi, this feature is taught, where in column 17 lines 66-67 and column 18 lines 1-5, and FIG.11 and FIG.25, Test Control Circuit 40 takes in TADD and outputs TADD to the Output Selection Circuit 84 that supplies the TOSEL<31:0> addresses (in this case 8 addresses) under control of the clock. It is obvious to the examiner that the Test Mode Detection Circuit 72 must latch the base address TADD that is then passed into the Output Selection Control Circuit for sequential addressing through 8 word addresses. And Haraguchi, in the Background, an advantage of the invention is the capability to detect certain types of single cell faults such as soft errors. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to apply the teachings of Haraguchi (scrambling expected data), including a test address latch, to the test circuit of Kazuyuki in order to include more types of testing, including a test for soft errors.

As per Claims 6 and 2:

Kazuyuki further teaches the method/test circuit for a semiconductor memory device, according to claims 5 and 1, wherein the high-speed data generating circuit outputs 1 bit of the internal read data read from the storage unit in accordance with one of n number (4) of the internal addresses, which coincides with the latch address (TADD of Haraguchi) and is synchronized with the high-speed clock (see Example disclosure).

As per Claims 8 and 4:

Kazuyuki further teaches the method/test circuit for a semiconductor memory device, according to claims 5 and 1, wherein the high-speed data generating circuit generates n bits (4) of the internal write data by use of any one of a fourth data generating method of alternately repeating the values "0" and "1" in this order (see Example, line 11). And in view of the motivation previously stated, the claims are rejected.

As per Claim 9:

Haraguchi further teaches the test circuit for a semiconductor memory device, according to claim 5, wherein the high-speed address generating circuit includes an external address (FIG.25 TADD) fetch/latch circuit (FIG.25 72) and an internal address generating circuit (FIG.25 74), the external address fetch/latch circuit fetches the external address (TADD), latches the external address to be supplied to the high-speed data generating circuit as a latch address (it is obvious to the examiner that the Test Mode Detection Circuit 72 must latch the base address TADD that is then passed into the Output Selection Control Circuit for sequential addressing through 8 word addresses) and transfers the fetched external address (TADD) to the internal address generating circuit (FIG.25 74), and the internal address generating circuit generates, in synchronization with the high-speed clock (FIG.5 TCLK), n number (in this case 8) of the internal addresses including the external address supplied from the external address fetch/latch circuit (see column 25 lines 42-67 and column 26 lines 1-34). And in view of the motivation previously stated, the claim is rejected.

16. Claims 7 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kazuyuki, Japanese Patent Application No. 07-078495, in view of Haraguchi et al. (herein Haraguchi), U.S. Patent No. 6650583 as applied to Claims 1 and 5 above, and further in view of Nomura et al. (herein Nomura). Kazuyuki and Haraguchi failed to further teach that which Nomura discloses, the method/test circuit for a semiconductor memory device, according to claims 5 and 1, wherein the high-speed address generating circuit includes any one of first address generating means for generating the internal addresses (TADD of Haraguchi) by sequentially increasing an address of the external address. Such an address increment model is shown in Nomura, FIG.6 and 14, where the address at each increment of a March algorithm is modified where the internal addresses are generated, and where n=1 in this case. And Nomura, in the Background, cites an advantage to be a self-test system to run burn-in tests without the requirement of an LSI Tester. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to include the self-test circuit of Nomura with the system of Kazuyuki and Haraguchi in order to add the capability of low cost burn-in testing.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2138

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